Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) A timing generator for use within a video processing device, comprising:

a random access memory;

a plurality of microsequencers coupled to said random access memory that produce flags based on programs stored in said random access memory; and

a programmable combinational logic module, coupled to said plurality of microsequencers that generates control signals based on the flags produced by said plurality of microsequencers to support a copy protection process.

2. (original) The timing generator of claim 1, further comprising:

a plurality of shift registers, coupled to said plurality of microsequencers that provide operating parameters to said plurality of microsequencers.

3. (original) The timing generator of claim 1, further comprising:

a means for downloading software changes to said timing generator while said timing generator is processing a video signal without substantial interference to a video signal being processed.

4. (original) The timing generator of claim 1, further comprising:

an instruction set that enables said plurality of microsequencers to share said random access memory.

5. (original) The timing generator of claim 1, wherein said plurality of microsequencers includes between two and ten microsequencers.

6. (original) The timing generator of claim 5, wherein said plurality of microsequencers includes seven microsequencers.

7. (cancelled)

8. (cancelled)

9. (original) The timing generator of claim 1, wherein said video processing device is a television.

10. (original) The timing generator of claim 1, wherein said video processing device is a cable set-top box.

11. (original) A video processing system, comprising:

a video input interface;

a video decoder coupled to said video input interface;

a video and graphics processor coupled to said video decoder;

a video encoder coupled to said video and graphics processor; and

a video output interface coupled to said video encoder,

wherein said video encoder includes a timing generator.

12. (cancelled)

13. (original) A video processing system of claim 11, wherein said video processing system has been implemented on a single integrated circuit.

14. (currently amended) A method for generating a time-dependent control signal for video signals, comprising the steps of:

(a) storing a plurality of programs within a random access memory;

(b) accessing a plurality of programs stored within the random access memory;

(c) executing a set of programs from said plurality of programs by a plurality of microsequencers to generate a set of flags;

(d) generating a control signal based on the set of flags through application of programmable ~~controlled~~ combinational logic; and

(e) outputting said control signal to implement a copy protection process.

15. (original) The method of claim 14, wherein the step of accessing includes arbitrating the access to the random access memory by the plurality of microsequencers.

16. (original) The method of claim 14, wherein the step of executing is completed in parallel by a plurality of microsequencers.

17. (cancelled)

18. (original) The method of claim 14, wherein the control signal is a horizontal sync control signal.

19. (original) The method of claim 14, wherein the control signal is an external horizontal sync control signal.

20. (original) The method of claim 14, wherein the control signal is an external vertical sync control signal.

21. (original) The method of claim 14, wherein the control signal is a vertical blanking active control signal.

22. (original) The method of claim 14, wherein the control signal is a color burst control signal.

23. (currently amended) The method of claim 14, wherein the control signal is a U Flip control signal ~~to generate MACROVISION color stripes~~.

24. (currently amended) The method of claim 14, wherein the control signal is a V Flip control signal ~~to generate MACROVISION color stripes~~.

25. (original) The method of claim 14, wherein the control signal is a vertical sync control signal.

26. (original) The method of claim 14, wherein the control signal is a vertical blank control signal.